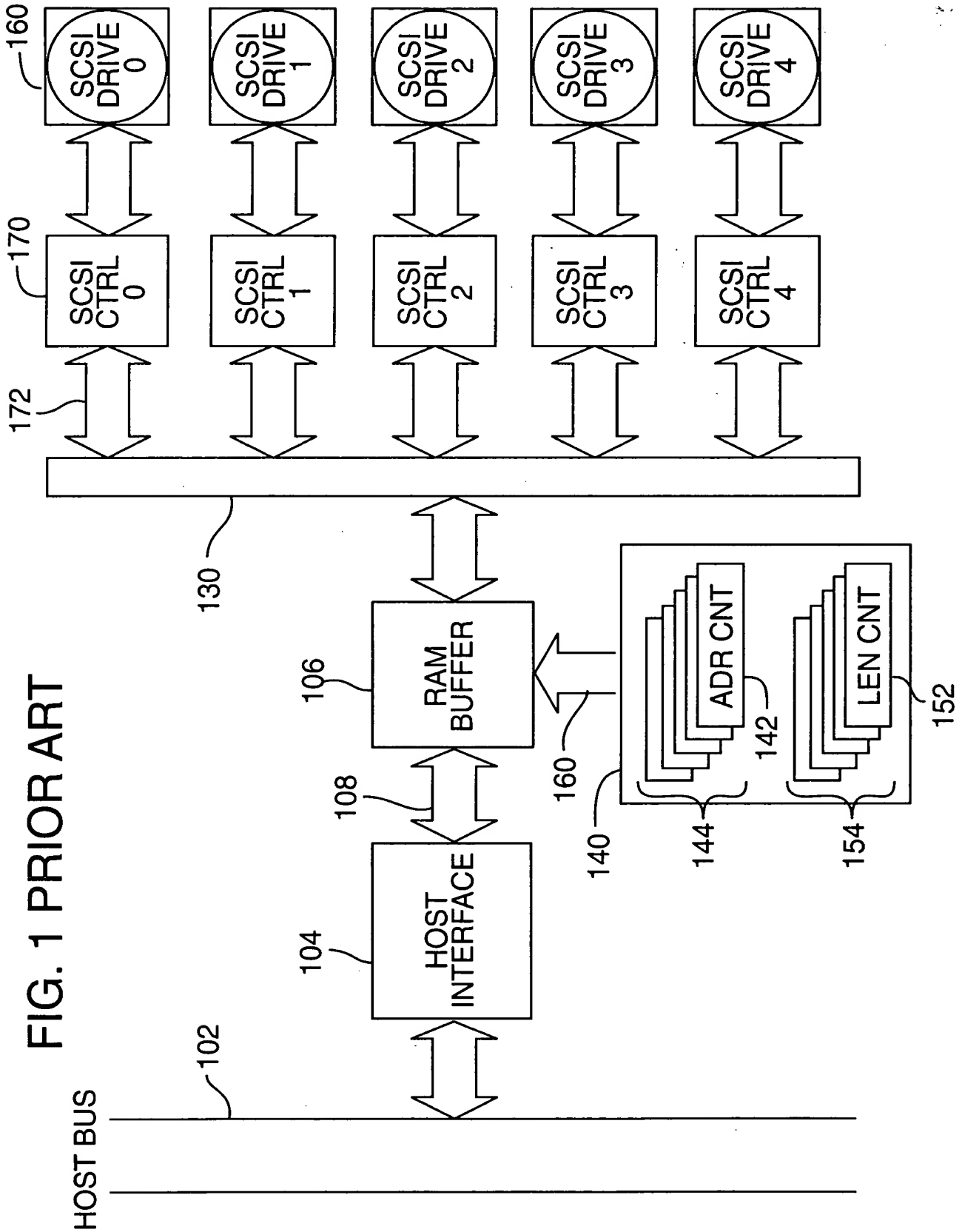


FIG. 1 PRIOR ART

FIG. 2

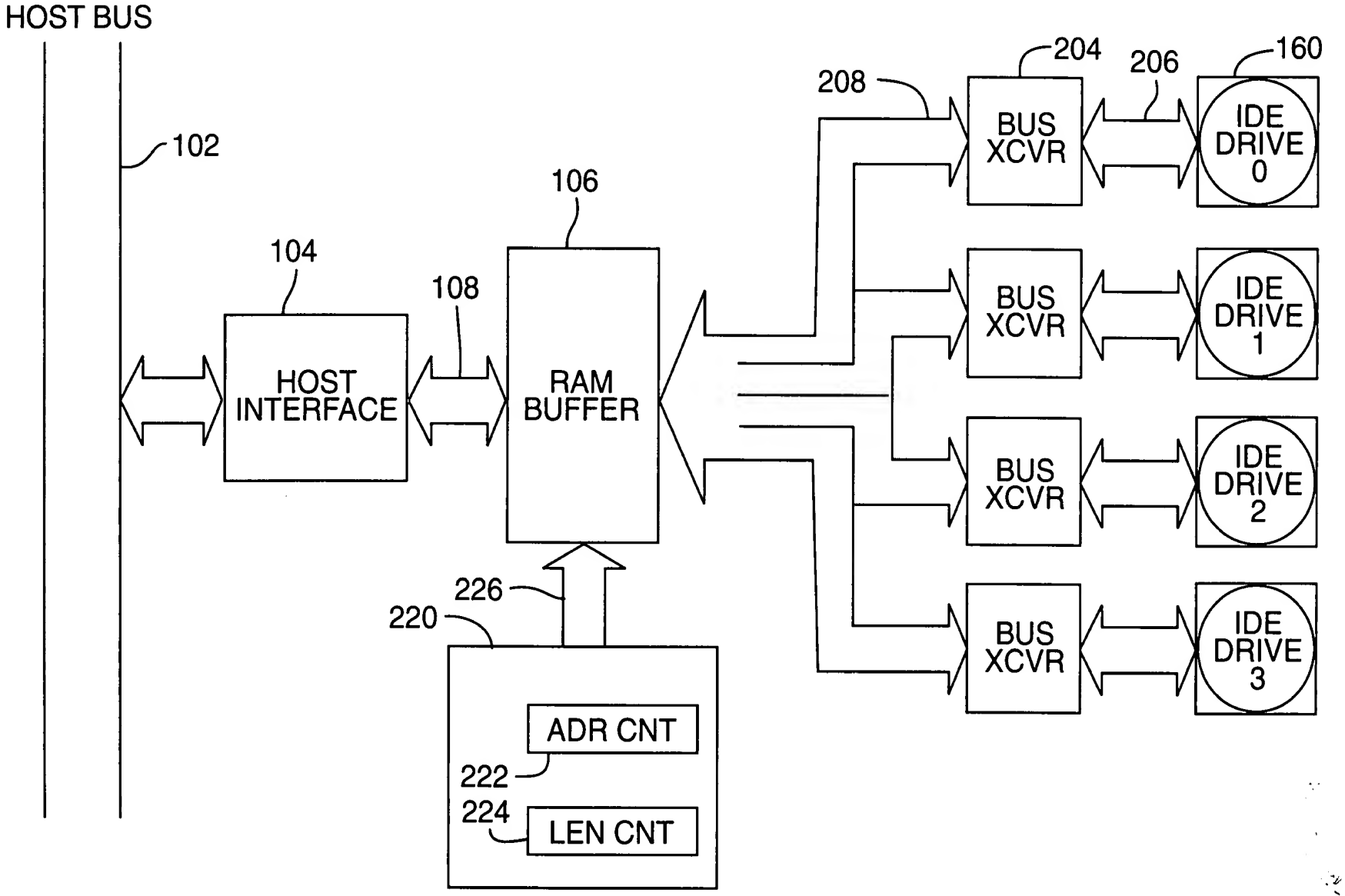

HOST BUS
102
104
HOST INTERFACE
108
106
RAM BUFFER
208
204
206
160
BUS XCVR
IDE DRIVE 0
BUS XCVR
IDE DRIVE 1
BUS XCVR
IDE DRIVE 2
BUS XCVR
IDE DRIVE 3
226
220
ADR CNT
222
224
LEN CNT

FIG. 3

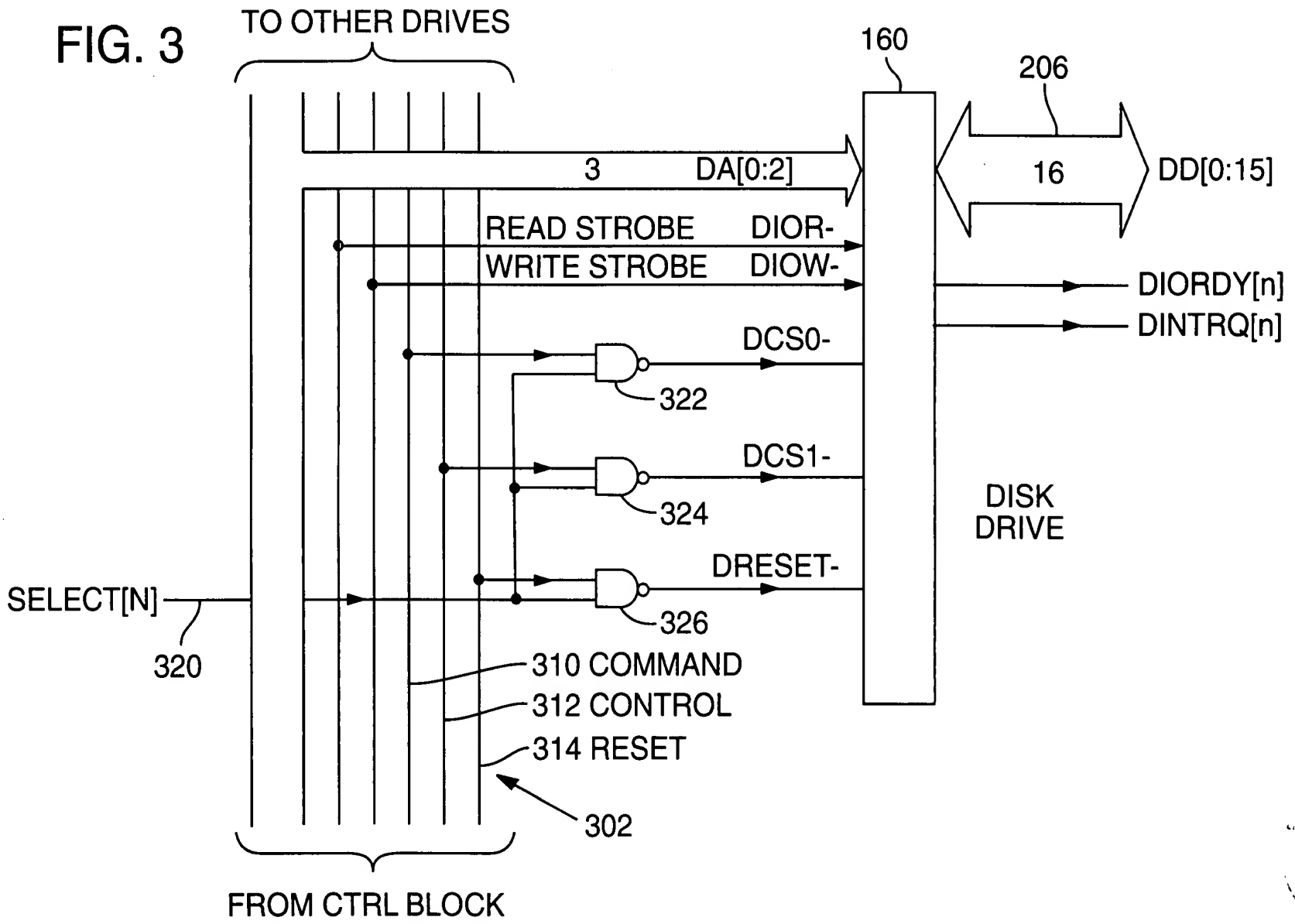

TO OTHER DRIVES
160
206
3
DA[0:2]
16
DD[0:15]
READ STROBE
DIOR-
WRITE STROBE
DIOW-
DIORDY[n]
DINTRQ[n]
DCS0-
322
DCS1-
324
DISK
DRIVE
DRESET-
326
SELECT[N]
320
310 COMMAND
312 CONTROL
314 RESET
302
FROM CTRL BLOCK

FIG. 4A

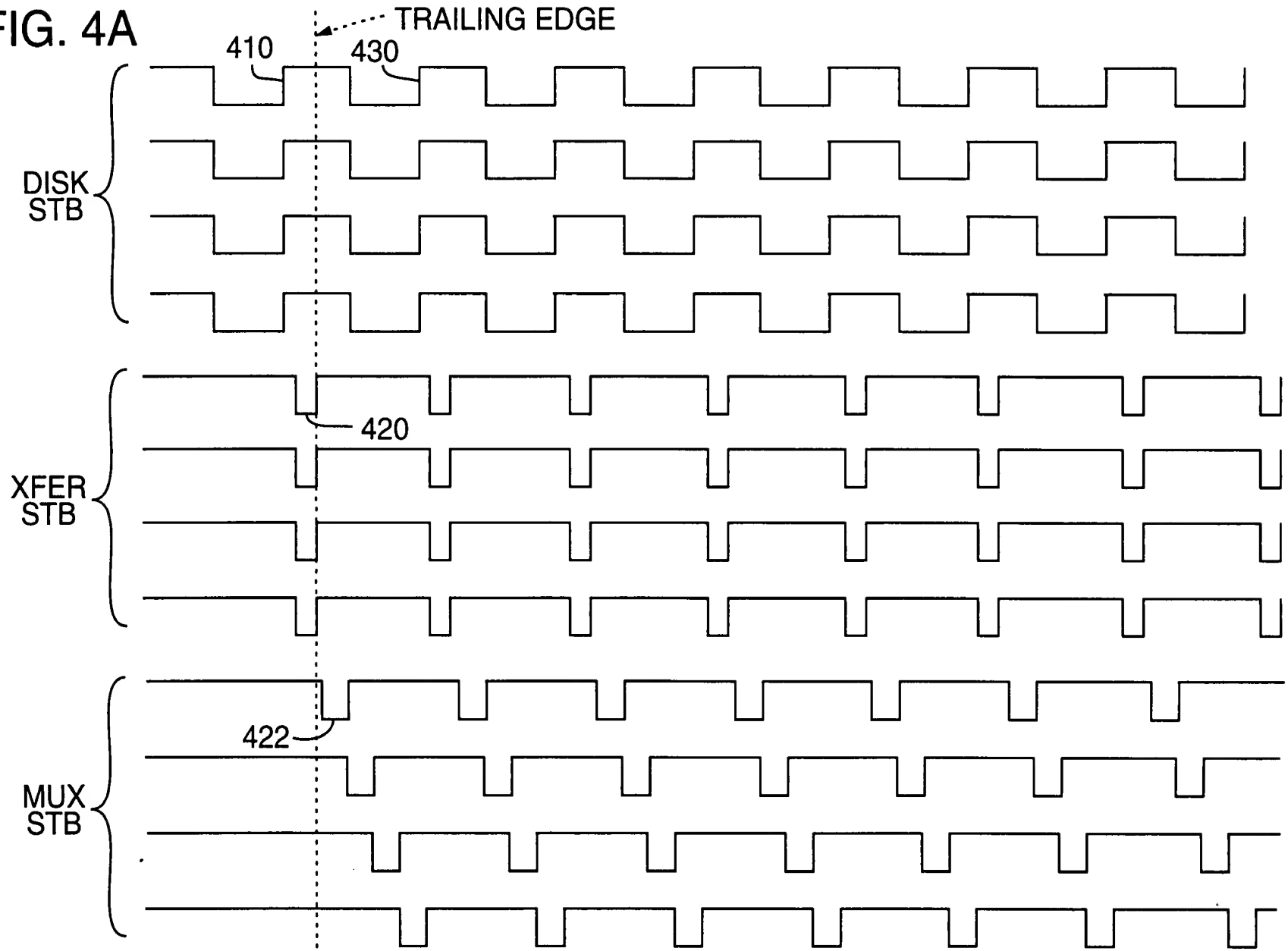


FIG. 4B

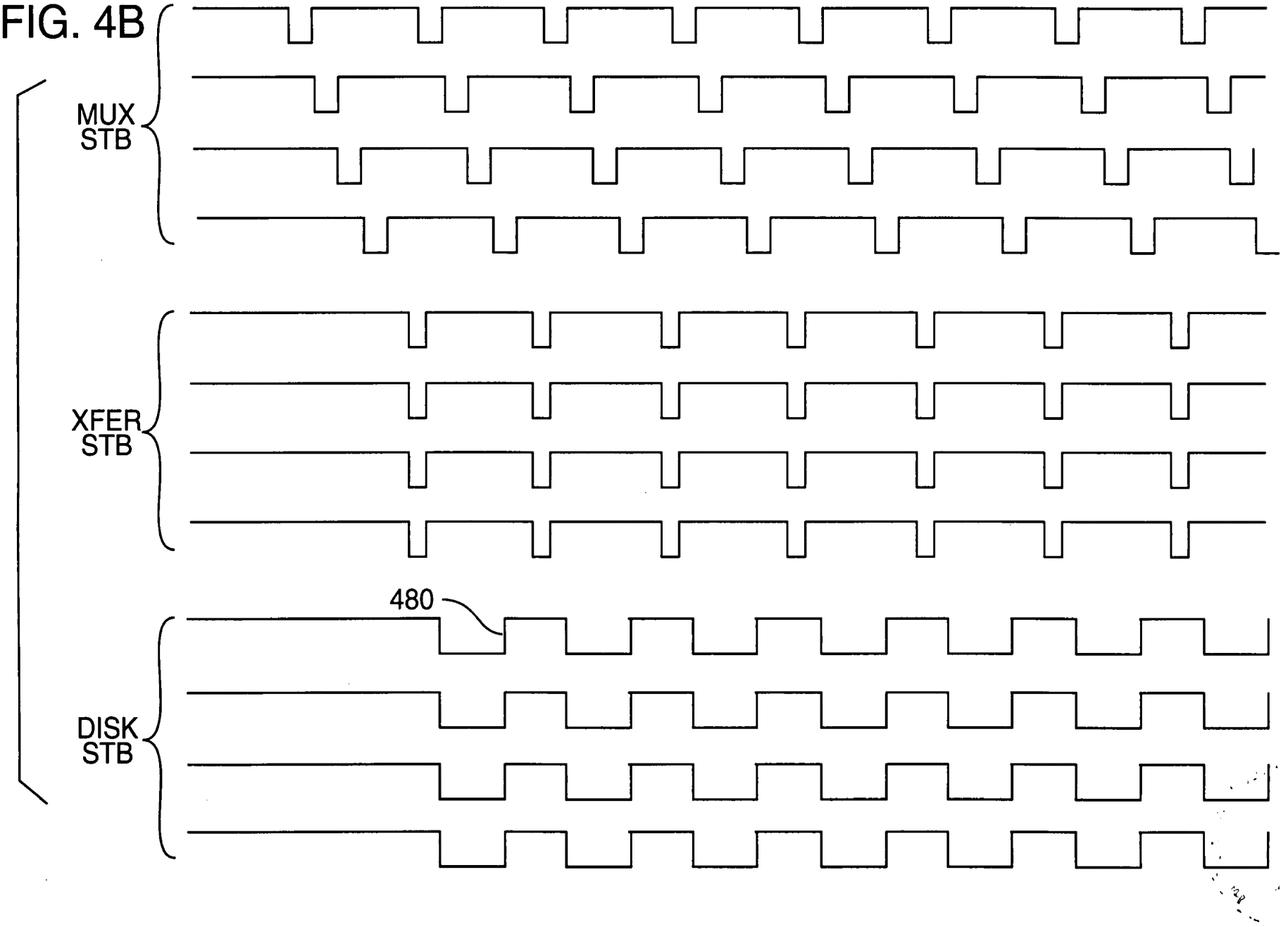


FIG. 5

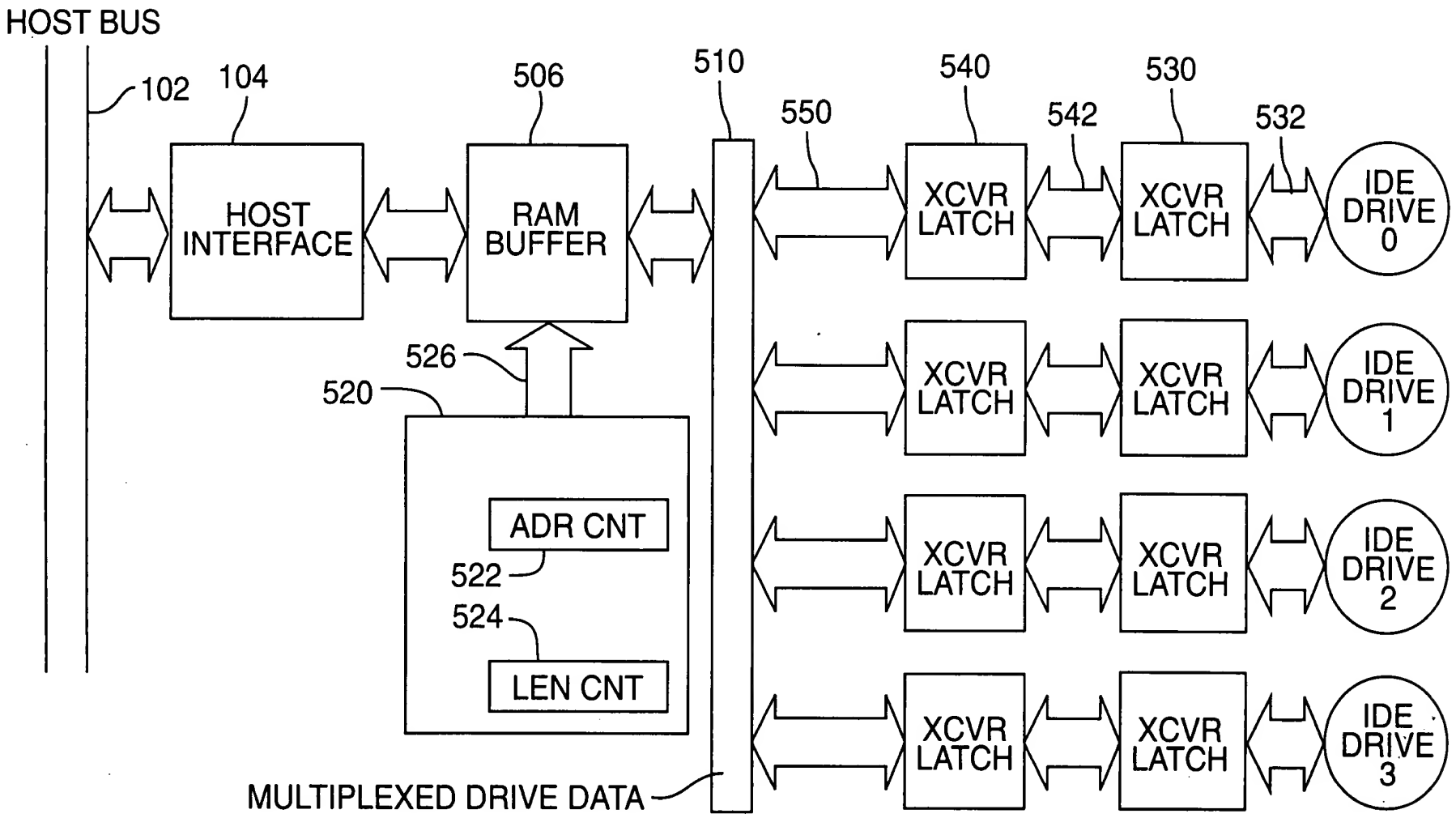
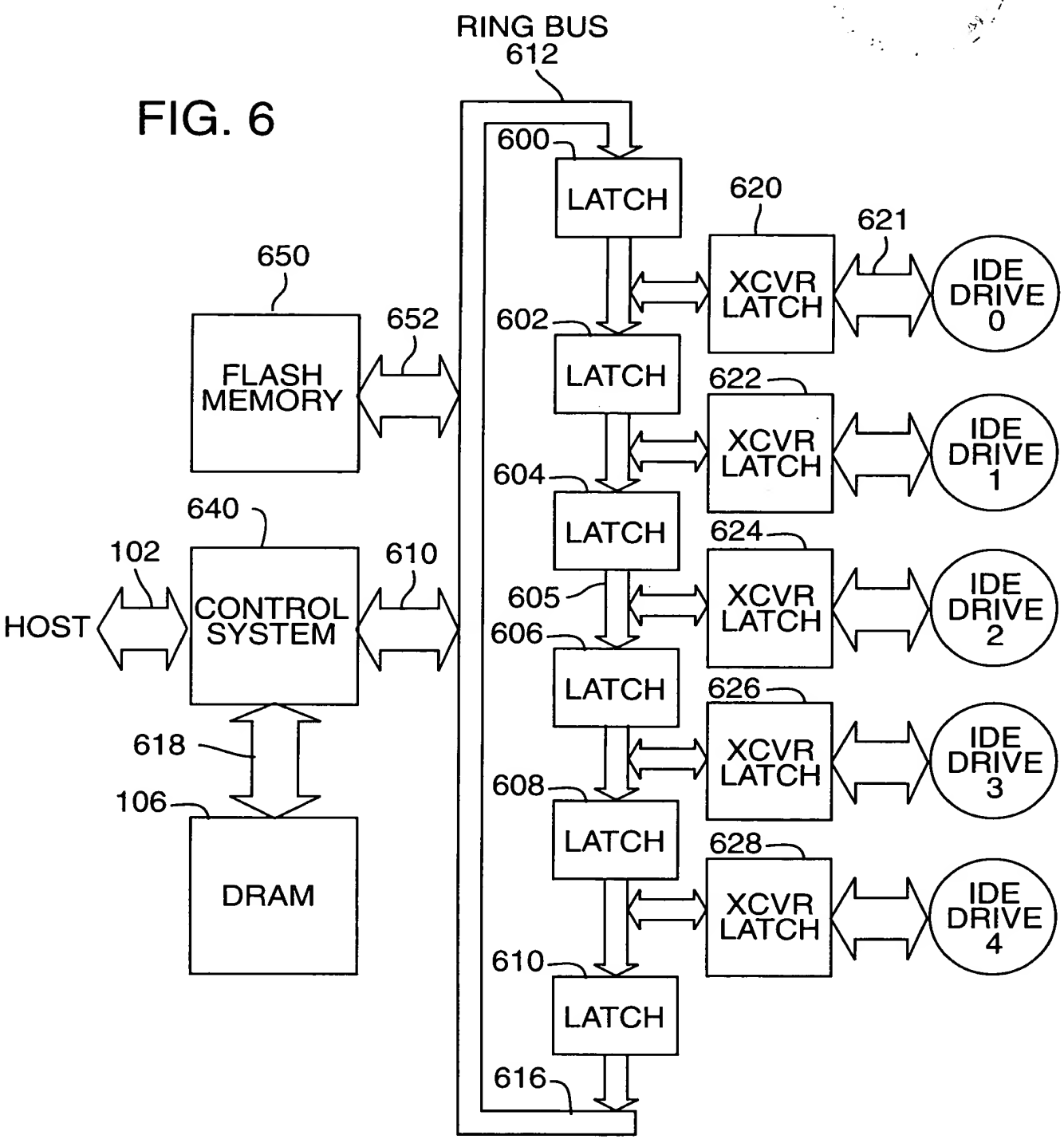

HOST BUS
102
104
506
510
550
540
542
530
532
HOST INTERFACE
RAM BUFFER
XCVR LATCH
XCVR LATCH
IDE DRIVE 0
526
520
XCVR LATCH
XCVR LATCH
IDE DRIVE 1
ADR CNT
522
524
LEN CNT
XCVR LATCH
XCVR LATCH
IDE DRIVE 2
XCVR LATCH
XCVR LATCH
IDE DRIVE 3
MULTIPLEXED DRIVE DATA

FIG. 6


RING BUS
612
600
LATCH
620
621
XCVR LATCH
IDE DRIVE 0
650
652
FLASH MEMORY
602
LATCH
622
XCVR LATCH
IDE DRIVE 1
604
LATCH
624
XCVR LATCH
IDE DRIVE 2
640
102
610
HOST
CONTROL SYSTEM
605
606
LATCH
626
XCVR LATCH
IDE DRIVE 3
618
608
106
LATCH
628
XCVR LATCH
IDE DRIVE 4
DRAM
610
LATCH
616

SYNCHRONOUS DATA TRANSFER

FIG. 7

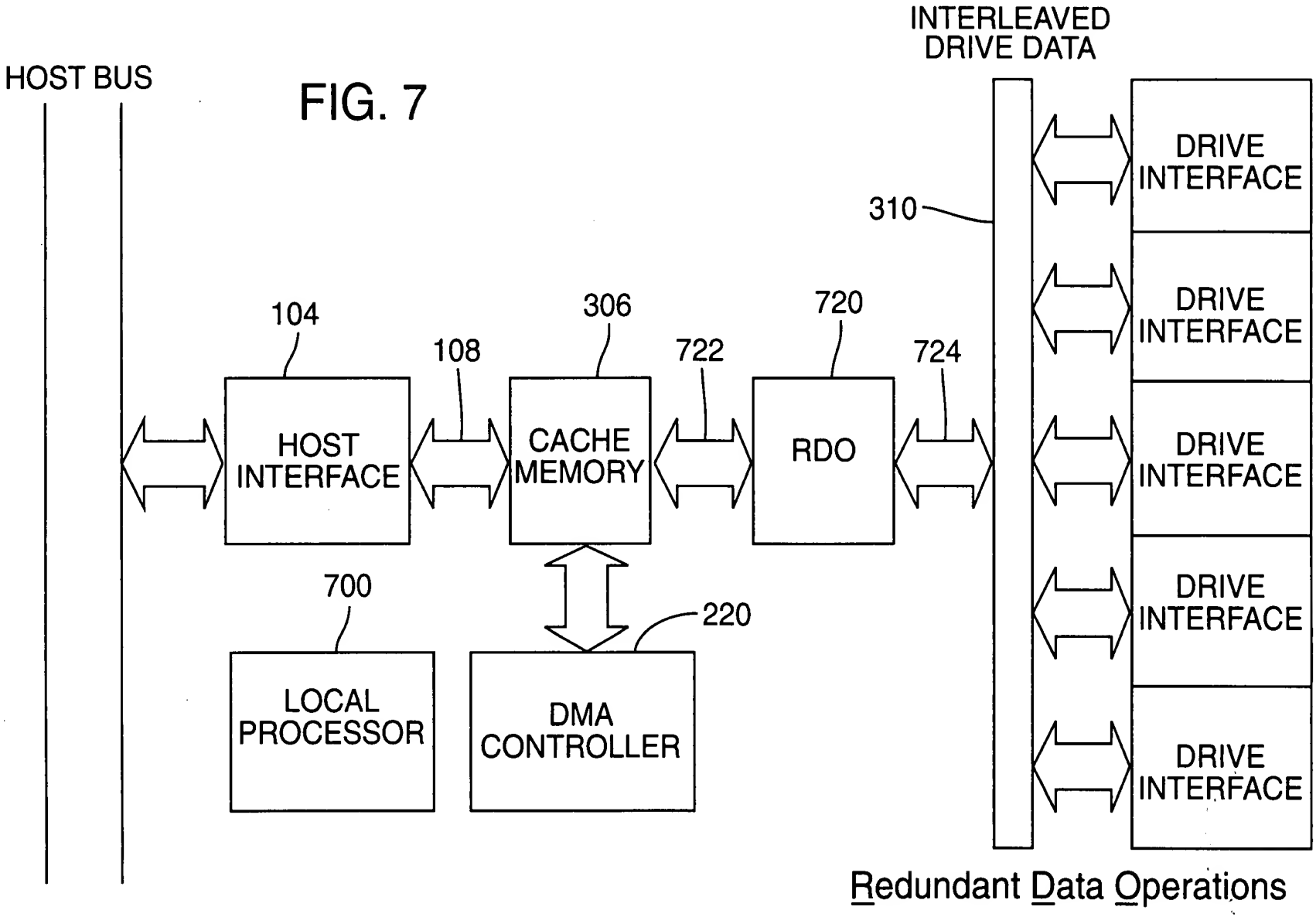


FIG. 8

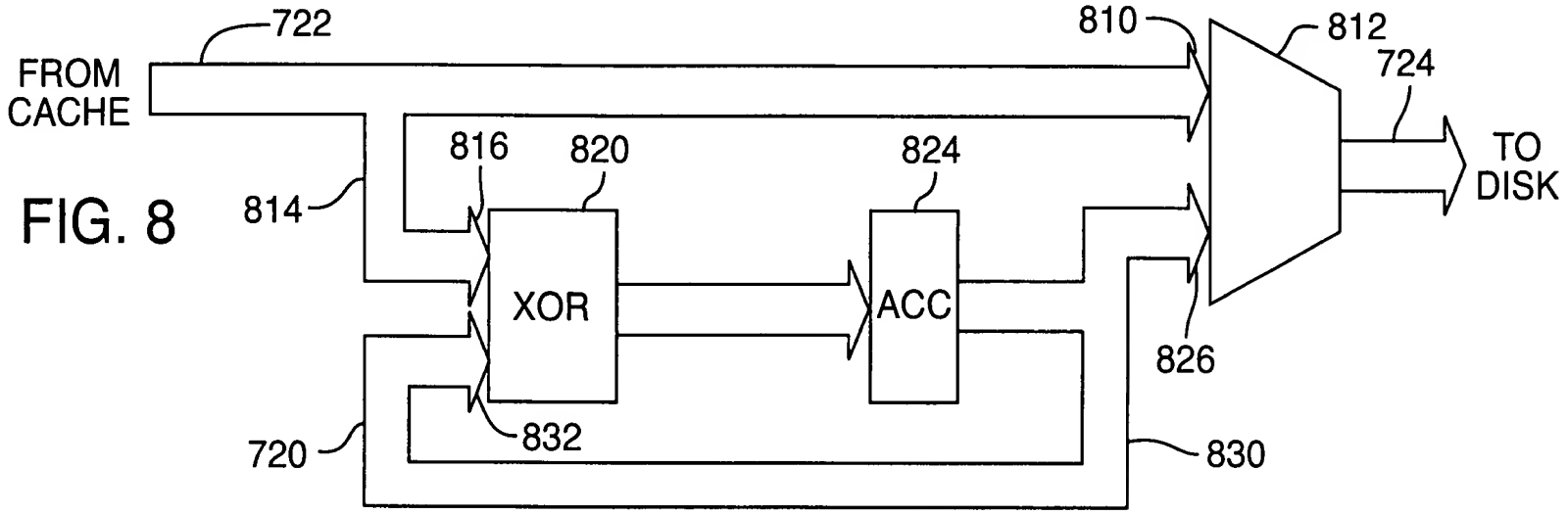

722
FROM CACHE
810
812
724
TO DISK
816
820
824
814
XOR
ACC
826
720
832
830

FIG. 9

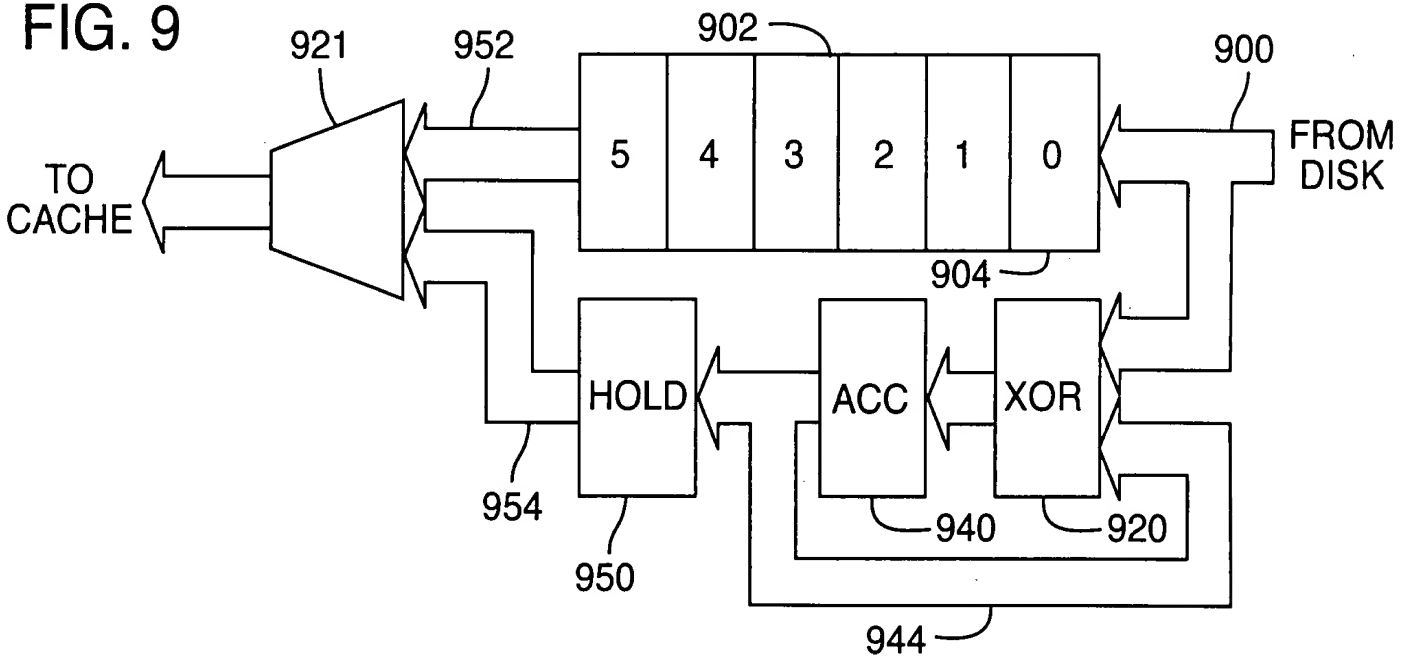

902
921
952
900
TO CACHE
5
4
3
2
1
0
FROM DISK
904
HOLD
ACC
XOR
954
940
920
950
944

FIG. 10

DISK READ - NO CORRECTION

		ACCUMULATOR(940)		HOLD	PIPELINE(902)						
State	INPUT	FUNCT	CONTENTS	LATCH							OUTPUT
0	A0	LOAD	A0		A0						
1	B0	XOR	A0+B0		B0	A0					
2	C0	XOR	A0+B0+C0		C0	B0	A0				
3	D0	XOR	A0+B0+C0+D0		D0	C0	B0	A0			
4	E0	XOR	A0+B0+C0+D0+E0		E0	D0	C0	B0	A0		
0	A1	LOAD	A1	A0+B0+C0+D0+E0	A1	E0	D0	C0	B0	A0	
1	B1	XOR	A1+B1	A0+B0+C0+D0+E0	B1	A1	E0	D0	C0	B0	A0
2	C1	XOR	A1+B1+C1	A0+B0+C0+D0+E0	C1	B1	A1	E0	D0	C0	**B0**
3	D1	XOR	A1+B1+C1+D1	A0+B0+C0+D0+E0	D1	C1	B1	A1	E0	D0	C0
4	E1	XOR	A1+B1+C1+D1+E1	A0+B0+C0+D0+E0	E1	D1	C1	B1	A1	E0	D0
0				A1+B1+C1+D1+E1		E1	D1	C1	B1	A1	
1				A1+B1+C1+D1+E1			E1	D1	C1	B1	A1
2				A1+B1+C1+D1+E1				E1	D1	C1	**B1**
3				A1+B1+C1+D1+E1					E1	D1	C1
4				A1+B1+C1+D1+E1						E1	D1

FIG. 11 DISK READ - WITH CORRECTION

		ACCUMULATOR(940)		HOLD							
State	INPUT	FUNCT	CONTENTS	LATCH	PIPELINE(902)						OUTPUT
0	A0	LOAD	A0		A0						
1	(xxx)	HOLD	A0		(xxx)	A0					
2	C0	XOR	A0+C0		C0	(xxx)	A0				
3	D0	XOR	A0+C0+D0		D0	C0	(xxx)	A0			
4	E0	XOR	A0+C0+D0+E0		E0	D0	C0	(xxx)	A0		
0	A1	LOAD	A1	A0+C0+D0+E0	A1	E0	D0	C0	(xxx)	A0	
1	(xxx)	HOLD	A1	A0+C0+D0+E0	(xxx)	A1	E0	D0	C0	(xxx)	A0
2	C1	XOR	A1+C1	A0+C0+D0+E0	C1	(xxx)	A1	E0	D0	C0	**B0**
3	D1	XOR	A1+C1+D1	A0+C0+D0+E0	D1	C1	(xxx)	A1	E0	D0	C0
4	E1	XOR	A1+C1+D1+E1	A0+C0+D0+E0	E1	D1	C1	(xxx)	A1	E0	D0
0				A1+C1+D1+E1		E1	D1	C1	(xxx)	A1	
1				A1+C1+D1+E1			E1	D1	C1	(xxx)	A1
2				A1+C1+D1+E1				E1	D1	C1	**B1**
3				A1+C1+D1+E1					E1	D1	C1
4				A1+C1+D1+E1						E1	D1

FIG. 12

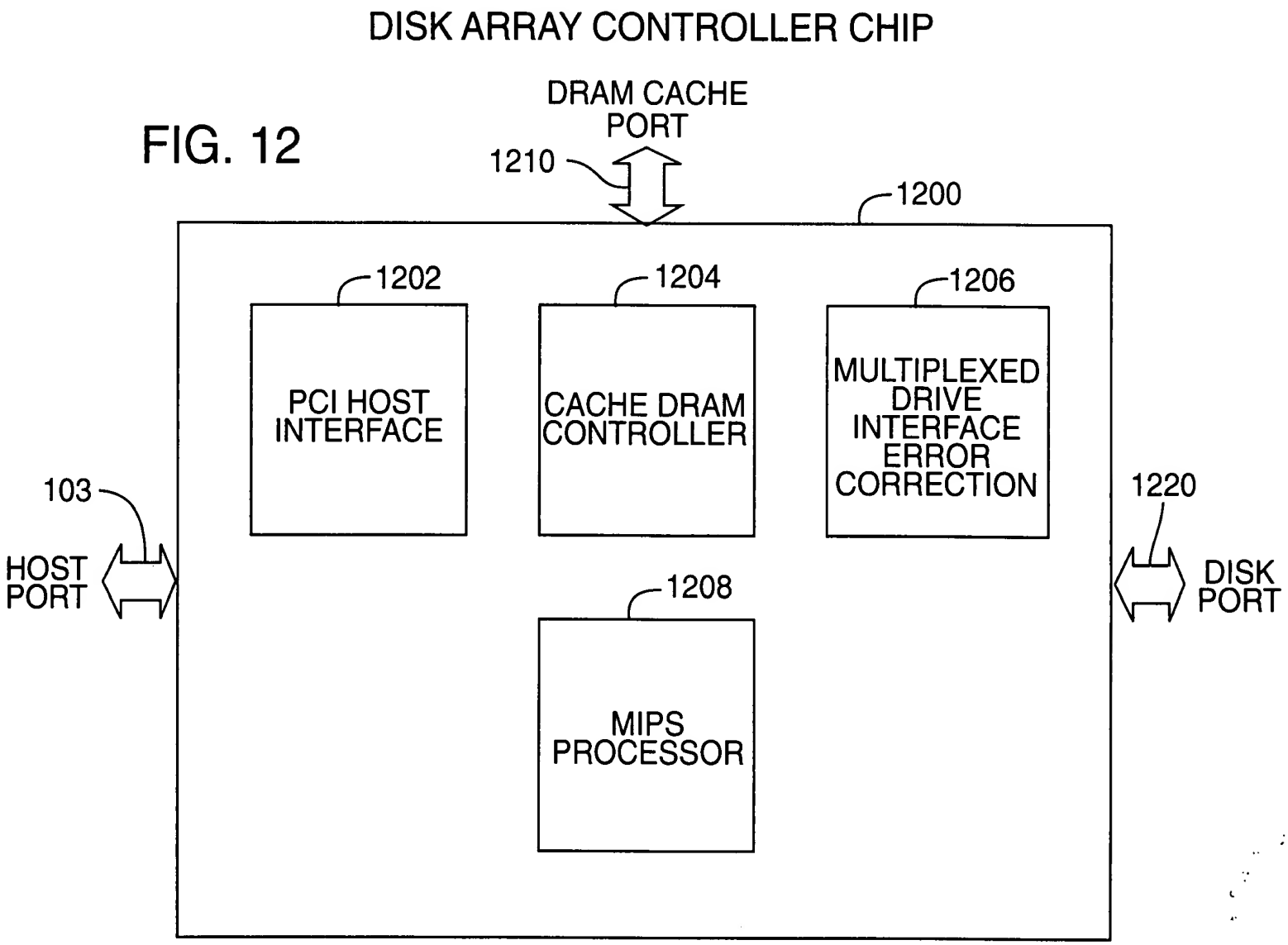

DISK ARRAY CONTROLLER CHIP
DRAM CACHE PORT
1210
1200
1202
PCI HOST INTERFACE
1204
CACHE DRAM CONTROLLER
1206
MULTIPLEXED DRIVE INTERFACE ERROR CORRECTION
103
HOST PORT
1220
DISK PORT
1208
MIPS PROCESSOR

FIG. 13

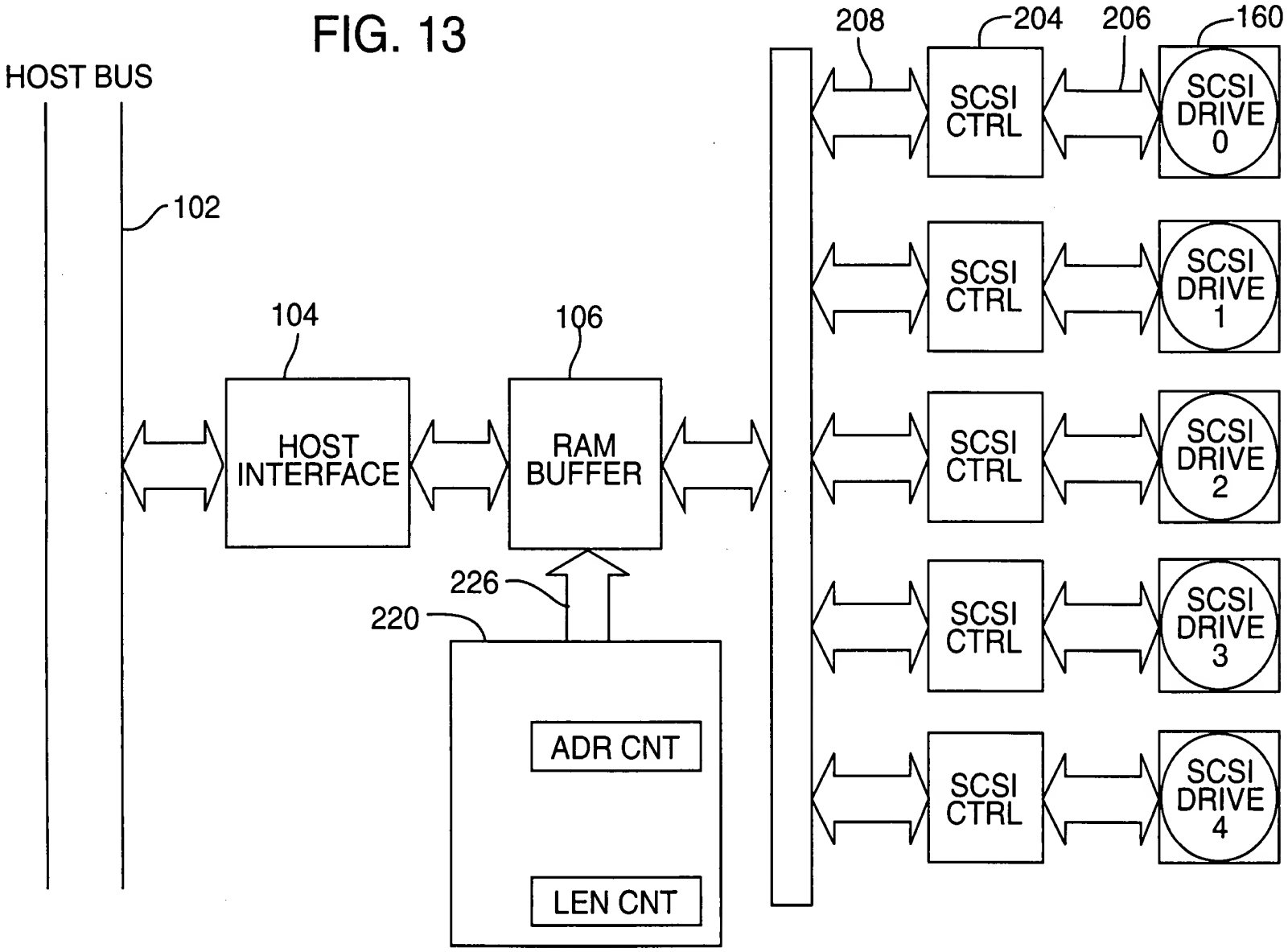

HOST BUS
102
104
HOST INTERFACE
106
RAM BUFFER
226
220
ADR CNT
LEN CNT
208
204
206
160
SCSI CTRL
SCSI DRIVE 0
SCSI CTRL
SCSI DRIVE 1
SCSI CTRL
SCSI DRIVE 2
SCSI CTRL
SCSI DRIVE 3
SCSI CTRL
SCSI DRIVE 4

FIG. 14